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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/885,784	06/20/2001	Mong-Song Liang	67,200-327	3661

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EXAMINER

MALDONADO, JULIO J

ART UNIT PAPER NUMBER

2823

DATE MAILED: 07/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/885,784

Applicant(s)

LIANG ET AL.

Examiner

Julio J. Maldonado

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 31 May 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-8 and 11-15 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8 and 12-15 is/are rejected.
- 7) ☒ Claim(s) 11 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s) \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

1. Applicant's cancellation to claims 9-11 is acknowledged. Claims 14 and 15 are newly added. Thus, claims 1-8 and 12-15 are pending in this application.

#### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 3-7, and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelly et al. (U.S. 6,143,117) in view of Haq (U.S. 6,245,677).

In reference to claim 1 Kelly et al. (Figs. 1-8) in a method to transfer thin film structures teach the steps of providing a first semiconductor substrate (40); forming over the first semiconductor substrate (40) at least one microelectronic device (44) to form from the first semiconductor substrate (40) a partially fabricated semiconductor integrated circuit microelectronic fabrication (44, 46); providing a second substrate (10); forming over the second substrate (10), in inverted order, a dielectric isolated metallization pattern (20, 26, 32, 34, 36, 38) intended to mate with the partially fabricated semiconductor integrated circuit microelectronic fabrication (44, 46); laminating the partially fabricated semiconductor integrated circuit microelectronic fabrication (44, 46) with the second substrate (10) to mate the partially fabricated semiconductor integrated circuit microelectronic fabrication (44, 46) with the dielectric isolated metallization pattern (20, 26, 32, 34, 36, 38) to thus form a laminated

completely fabricated semiconductor integrated circuit microelectronic fabrication (44, 46, 20, 26, 32, 34, 36, 38); and removing the second substrate (10) from the laminated completely fabricated semiconductor integrated circuit microelectronic fabrication (44, 46, 20, 26, 32, 34, 36, 38) while employing a dicing method (column 4, line 55 – column 9, line 43).

Kelly et al. fail to teach removing the second substrate from the laminated completely fabricated semiconductor integrated circuit microelectronic fabrication while employing a method selected from the group consisting of milling methods, polish methods and chemical mechanical polish (CMP) planarizing method. However, Haq (Fig.1) in a related method to remove substrates teaches removing a substrate (step 4) using a method selected from the group consisting of milling methods, polish methods and chemical mechanical polish (CMP) planarizing method (column 2, line 55 – column 4, line 9).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to remove the substrate using the polishing method of Haq in the mounting method of Kelly et al., since by this manner this would reduce stress forces to the wafer during manufacturing (column 2, lines 66-67).

In reference to claims 3-6, and 12-13 Kelly et al. show that the second substrate (10) is selected from the group consisting of conductor substrates, semiconductor substrates and aggregates thereof; that the second substrate (10) is a second semiconductor substrate; that the first semiconductor substrate (40) is thicker than the second substrate (10); that the dielectric isolated metallization pattern (20, 26, 32, 34,

36, 38) comprises a plurality of laminated patterned conductor layers; that the mating of the partially fabricated semiconductor integrated circuit microelectronic fabrication (44, 46) with the dielectric isolated metallization pattern (20, 26, 32, 34, 36, 38) formed over the second substrate (10) is undertaken while employing a laminating method consisting of thermally assisted laminating; removing from the laminated completely fabricated semiconductor integrated circuit microelectronic fabrication (44, 46, 20, 26, 32, 34, 36, 38) the second substrate (10); that the semiconductor substrate is not thinned after forming thereover the minimum of one microelectronic device; and that the second substrate (10) is not removed from the dielectric isolated metallization pattern (20, 26, 32, 34, 36, 38) prior to mating the partially fabricated semiconductor integrated circuit microelectronic fabrication (44, 46) with the dielectric isolated metallization pattern (20, 26, 32, 34, 36, 38) (column 4, line 55 – column 9, line 43).

In reference to claim 7, Kelly et al. in combination with Haq show all aspects of the invention but fails to teach that each laminated patterned conductor layer within the plurality of laminated patterned conductor layers is formed to a thickness of from about 3,000 to about 6,000 Å. This claim is prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum

value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kelly et al. ('117) in view of Haq ('677) as applied to claims 1, 3-6, and 12-13 above, and further in view of Davidson (U.S. 5,880,010).

Kelly et al. in combination with Haq substantially teach all aspects of the invention but fail to teach that the microelectronic device is selected from the group consisting of resistors, transistors, diodes and capacitors. However, Davidson in a related method to form packaging structures teach that the microelectronic device (i.e. the active layer) is selected from the group consisting of resistors, transistors, diodes and capacitors (column 3, lines 58-67).

Therefore, it would have been obvious to skilled in the art at the time of the invention was made to incorporate the microelectronic devices as taught by Davidson in the packaging structure of Kelly et al. and Haq, since by integrating then it would reduce the space of an integrated circuit to less than 1% of its conventional size (column 1, lines 35-39).

5. Claims 8, 14 and 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Kelly et al. ('117) in view of Kresge et al (U.S. 6,066,808).

Kelly et al. (Figs. 1-8) teach a related method to transfer thin film structures including the steps of providing a first semiconductor substrate (40); forming over the first semiconductor substrate (40) at least one microelectronic device (44) to form from

the first semiconductor substrate (40) a partially fabricated semiconductor integrated circuit microelectronic fabrication (44, 46); providing a second substrate (10); forming over the second substrate (10), in inverted order, a dielectric isolated metallization pattern (20, 26, 32, 34, 36, 38) intended to mate with the partially fabricated semiconductor integrated circuit microelectronic fabrication (44, 46); and laminating the partially fabricated semiconductor integrated circuit microelectronic fabrication (44, 46) with the second substrate (10) to mate the partially fabricated semiconductor integrated circuit microelectronic fabrication (44, 46) with the dielectric isolated metallization pattern (20, 26, 32, 34, 36, 38) to thus form a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication (44, 46, 20, 26, 32, 34, 36, 38) (column 4, line 55 – column 9, line 43).

Kelly et al. fail to teach using thermally assisted laminating methods and pressure assisted lamination methods to mate the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern using a bonding material selected from the group consisting of indium and indium alloy bonding materials. However, Kresge et al. (Fig.11) in a related method to form multilayered circuit boards, teach using pressure and temperature lamination methods using a bonding material selected from the group consisting of indium and indium alloy bonding materials (column 7, line 45 – column 8, line 35). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use pressure bonding lamination using indium or indium alloy as bonding material as taught by Kresge et al. in the mounting method of Kelly et al., since this

would promote an effective engagement between the integrated circuits, and prevent dielectric intrusion through the conductive bond (column 8, lines 9-35).

***Allowable Subject Matter***

6. Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: Kelly et al. to U.S. 6,143,117 (Figs. 1-8) teach a related method to transfer thin film structures including the steps of providing a first semiconductor substrate (40); forming over the first semiconductor substrate (40) at least one microelectronic device (44) to form from the first semiconductor substrate (40) a partially fabricated semiconductor integrated circuit microelectronic fabrication (44, 46); providing a second substrate (10); forming over the second substrate (10), in inverted order, a dielectric isolated metallization pattern (20, 26, 32, 34, 36, 38) intended to mate with the partially fabricated semiconductor integrated circuit microelectronic fabrication (44, 46); laminating the partially fabricated semiconductor integrated circuit microelectronic fabrication (44, 46) with the second substrate (10) to mate the partially fabricated semiconductor integrated circuit microelectronic fabrication (44, 46) with the dielectric isolated metallization pattern (20, 26, 32, 34, 36, 38) to thus form a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication (44, 46, 20, 26, 32, 34, 36, 38); and removing the second substrate (10) from the laminated completely fabricated semiconductor integrated circuit microelectronic fabrication (44,



46, 20, 26, 32, 34, 36, 38) while employing a dicing method (column 4, line 55 – column 9, line 43). However, Kelly et al. neither teach nor suggest using the dielectric isolated metallization pattern as a stop layer for a CMP process.

8. Haq to U.S. U.S. 6,245,677 (Fig.1) in a related method to remove substrates teaches the step of removing a substrate (step 4) using a method selected from the group consisting of milling methods, polish methods and chemical mechanical polish (CMP) planarizing method (column 2, line 55 – column 4, line 9). However, Haq fails to teach using a dielectric isolated metallization pattern as a stop layer for a CMP process.

#### ***Response to Arguments***

9. Applicant's arguments with respect to claims 1-8 and 12-13 have been considered but are moot in view of the new ground(s) of rejection.

#### ***Conclusion***

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Papers related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2823 Fax Center number is **(703) 305-3432**. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Julio J. Maldonado** at **(703) 306-0098** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via [julio.maldonado@uspto.gov](mailto:julio.maldonado@uspto.gov). If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (703) 308-4918.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

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